



Advanced Non-Volatile Memories (NVM)

Jean Yang-Scharlotta

jean.yang-scharlotta@jpl.nssa.gov

818-354-0412

Jet Propulsion Laboratory –California Institute of Technology

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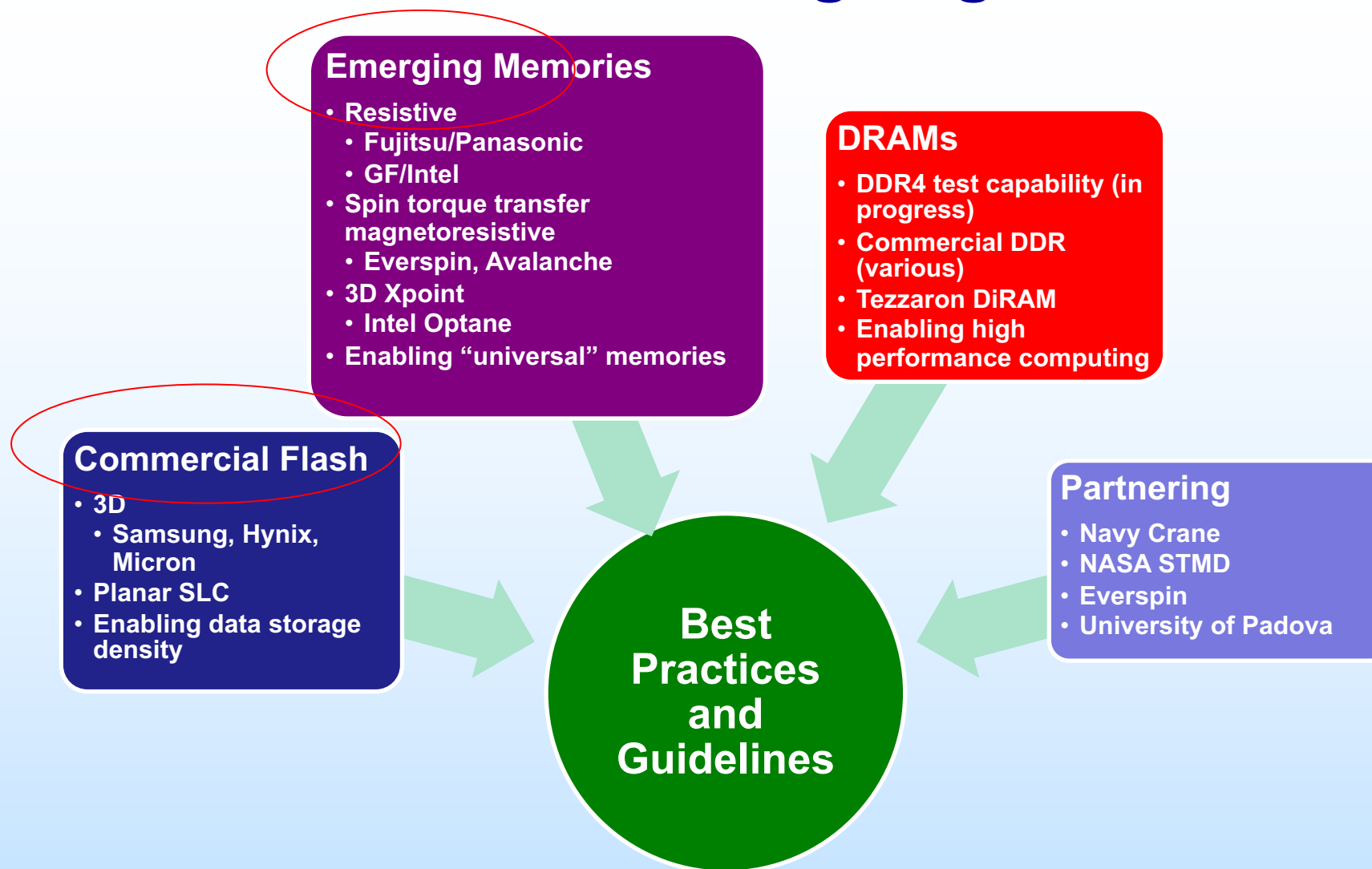


Outline

- **Introduction- Tracking and Evaluating Memory Technologies**
- **Roadmap Recent Testes and Planned Test**
- **Emerging Memory Update 2019**
 - **STT-MRAM**
 - **Future Plans**
- **NAND Flash Update 2019**
- **Summary**



NEPP – Memories Ongoing Activities





Commercial NVM Technology Roadmap

- collaborative with NSWC Crane, others

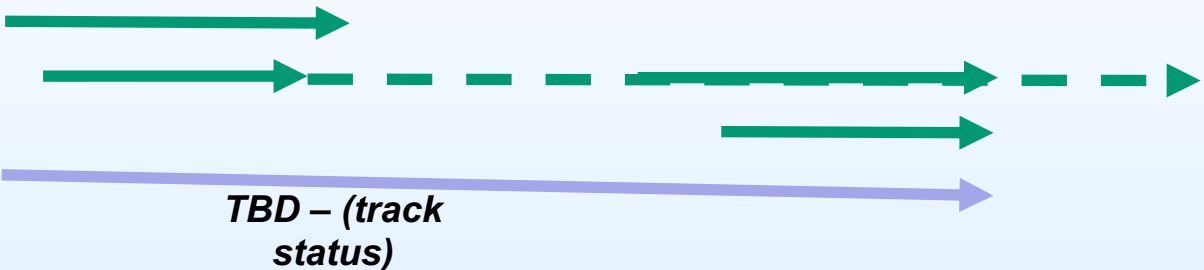
Other

- STT-MRAM (Avalanche, Everspin (STMD))
- FeRAM



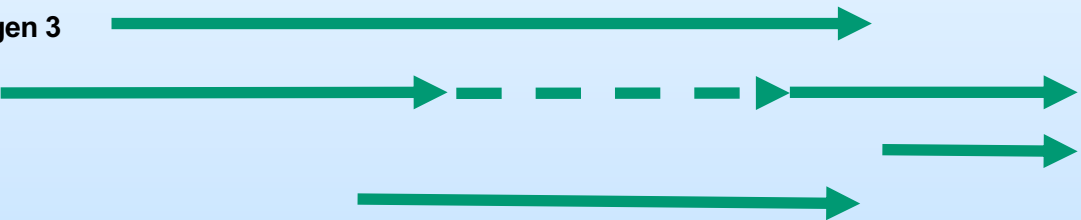
Resistive

- CBRAM (Adesto)
- ReRAM (Panasonic/Fujitsu)
- 3D XPoint (Intel Optane™)
- TBD (HP Labs, others)



NAND FLASH

- Samsung VNAND (gen 1, 2 – complete, gen 3 FY17)
- Micron planar (16nm)
- Micron 3D
- SK Hynix 3D, other





Emerging Memory in 2019

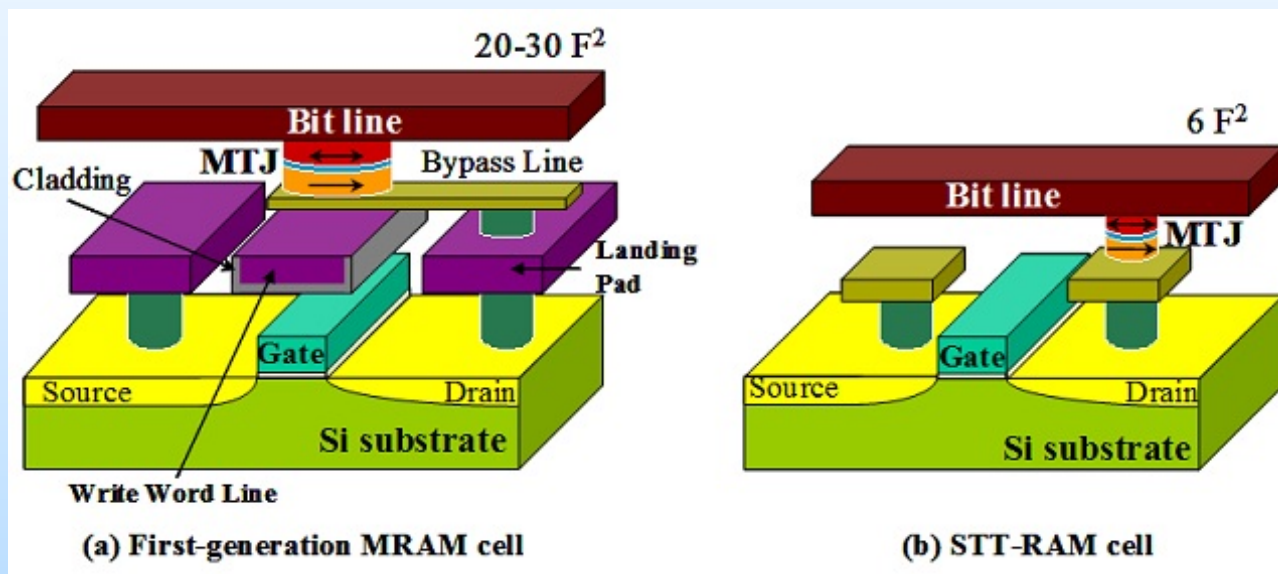
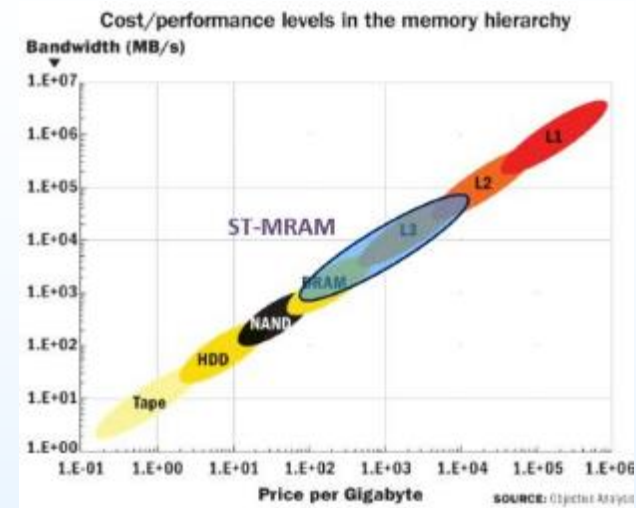
- **STT-MRAM gaining wide adoption as embedded flash replacement around 22-28nm nodes**
 - Intel announced p-STTMRAM production on 22nm FINFET technology in Feb (ISSCC)
 - Samsung announced e-STMRAM production on 28nm FDSOI technology in May
 - Global Foundries had previously reported that it plans to have STTMRAM as embedded memory in its 22nm technology
 - Also fabricating Everspin's 1Gb STTMRAM on its 28nm CMOS technology
 - UMC licenced 28nm STTMRAM from Avalanche
- **Memory has internal EDAC- should be considered in application**

–<https://www.mram-info.com/samsung-starts-shipping-28nm-embedded-mram-memory>



Spin Torque Transfer Magnetic Memory (STT-MRAM)

- STT-MRAM is a near term storage & working memory technology
 - MRAM already used in RH applications
- STT-MRAM enables further scaling of density well above current RH availability
- 256Mb chip in production 1Gb in sampling from Everspin





Spin Torque Transfer Magnetic Memory (STT-MRAM)

- **Everspin Technologies**



- 1st Gen MRAM in 16Mb products by Honeywell and Cobham
- New STT-MRAM **256Mb DDR3** chip targeting high speed and high density, 1Gb part coming soon
- Testing scheduled for STMD for FY18
- Of interest for **RH processor system memory**

Test Results (Guertin, RADECS 2018)

- Tests were done unbiased due to interest as candidate for Rad Hard memory part and shows memory core quite robust in radiation
- TID test show no data loss up to 1.5Mrad (Si) for the part
- TID testing on the memory cell show no bit flips up to 7Mrad(Si)
- SBU cross section $<1 \times 10^{-7} \text{cm}^2$ at LET 33.7 MeV-cm²/mg.

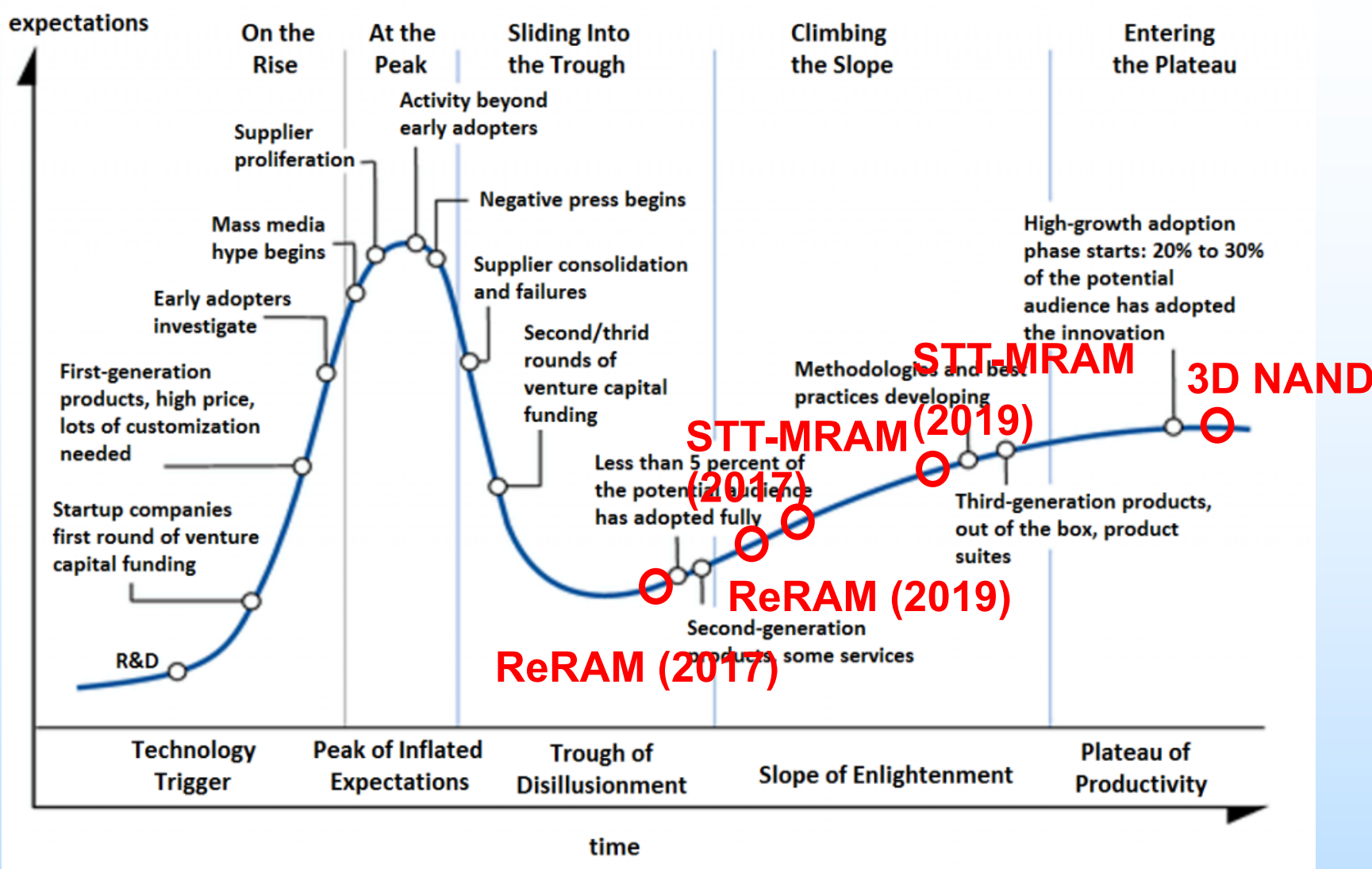


Emerging Memory Looking Forward

- The value of tracking commercial development through partnership is demonstrated, and continuing
- The duel study done for STTMRAM, where we include fundamental memory device testing and production part testing at the same time allowed for separation part level reliability and radiation performance (influenced by manufacturer dependent support circuitry design) from fundamental reliability of the memory core itself which should remain constant from manufacturer to manufacturer for the same device architecture.
 - Currently MRAM fundamental device study is on-going with University of Minnesota
- Technology Tracking and Testing in 2019 will continue to
 - Track the more mature STT-MRAM and test new products for potential use for agency-wide information gathering
 - Continue to track the also maturing RRAM, and other emerging memories as new products and architectures become available for testing



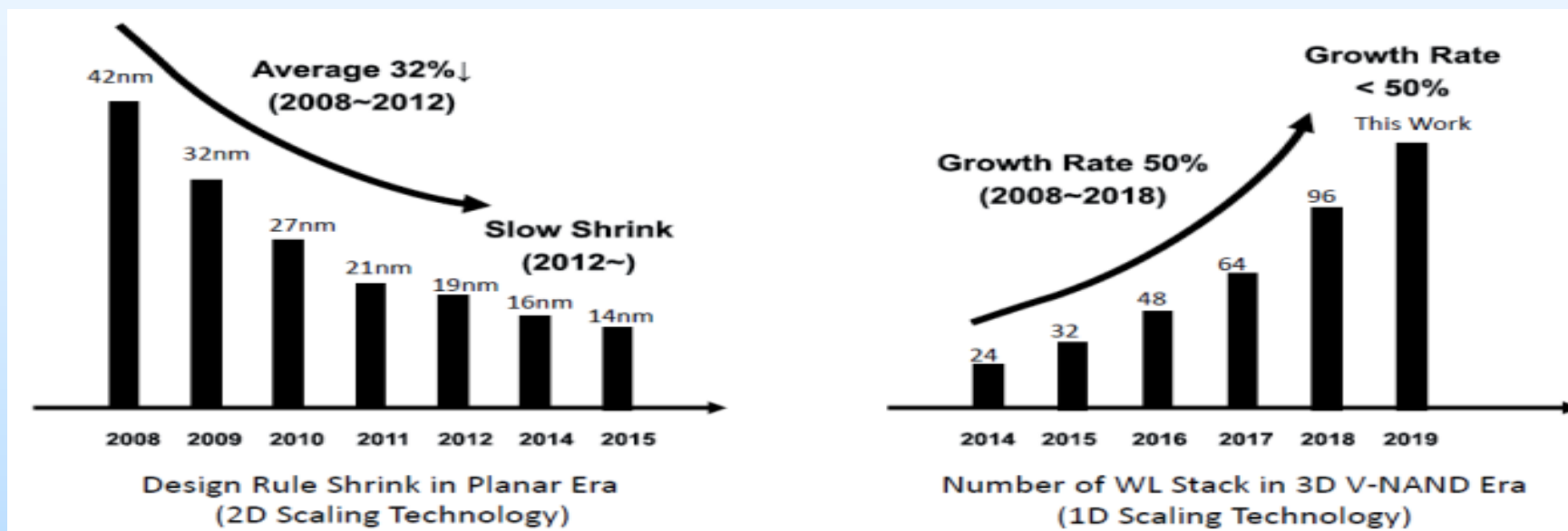
Diatribes: Gartner Hype Cycle Concept





NAND Flash in 2019

- **NAND Flash continues to move to 3D**
 - Very mature, bulk of NAND production
 - Scaling is by inc. # of stacks, now 96 or 128 layers
 - For leading manufacturer Samsung, 6th generation VNAND announced
- **Planar scaling has slowed down but availability is steady**
 - Automotive market sustaining high reliability SLC products



From ISSCC 2019,
Samsung



NAND Flash in 2019

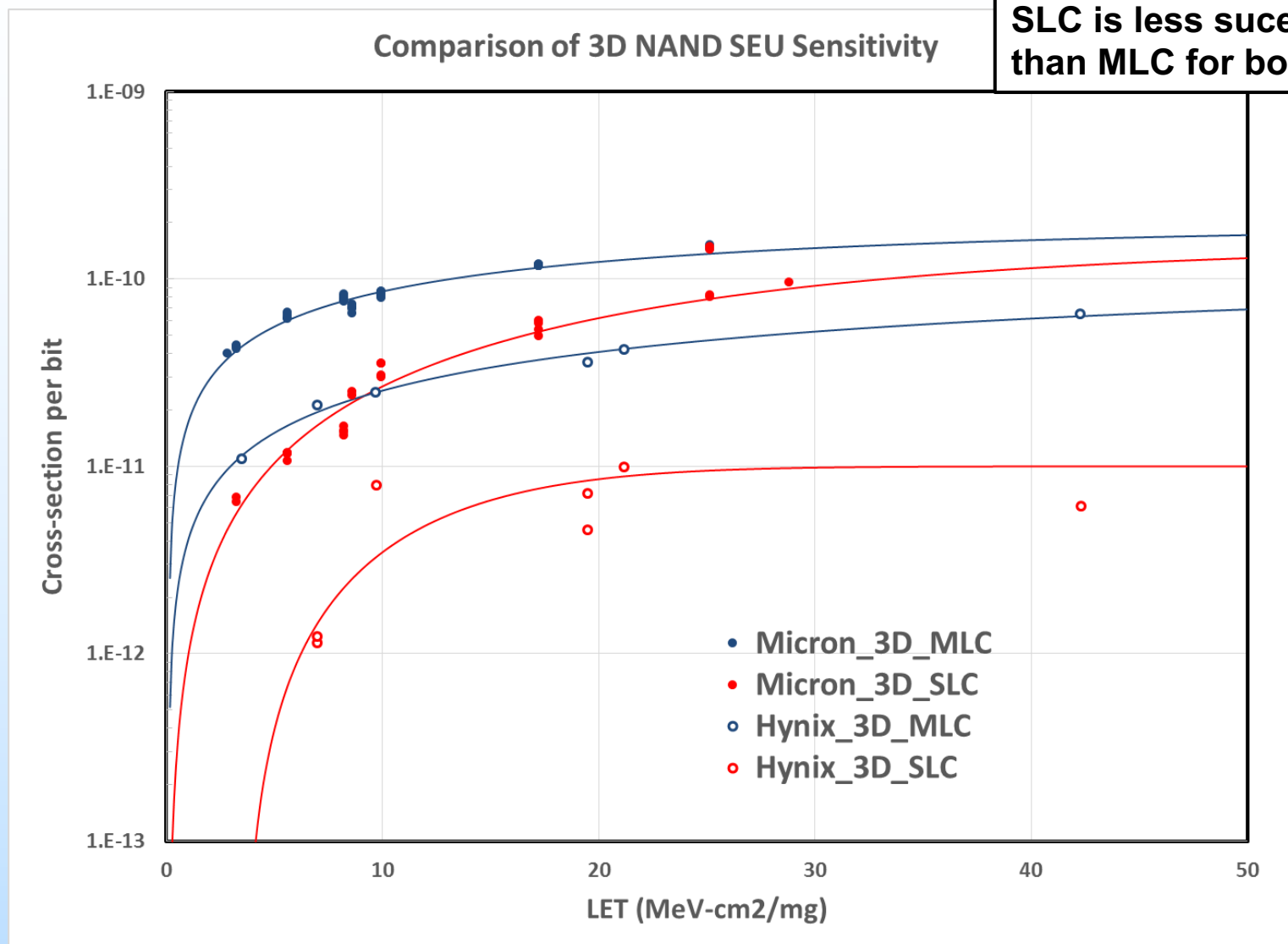
- **Implications of NAND Manufacturers Targeting the Automotive Market**
 - **More choices for high reliability parts**
 - High density SLC parts now available in planar and in 3D NAND SLC mode
 - Wider selection of densities, technologies and manufacturers available for high reliability needs
 - Versus managed NAND such as SSD, iNAND, eMMC, SD cards which dominate the market and manufacturer support. E.g. Samsung VNAND is only available as SSD
 - **Wider operating temperature available**
 - **More product longevity (>10 yr vs 2-4yrs)**
 - If we qualify a part, there is greater chance for reuse in future missions
 - Greater incentive for more thorough in evaluation of NAND

➤ **New NAND reliability eval tool**



3D NAND Static SEU Comparison:

—From this GSFC test we see that SLC is less susceptible to SEU than MLC for both manufacturer



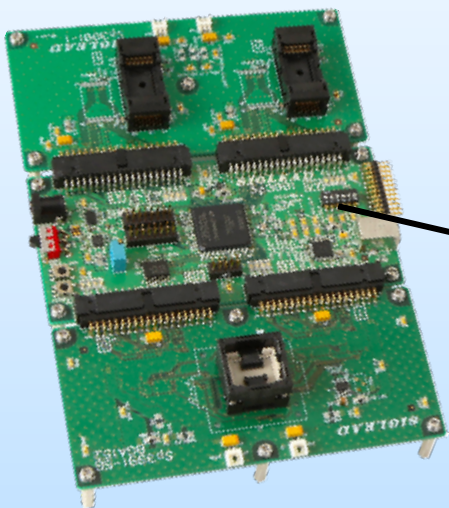
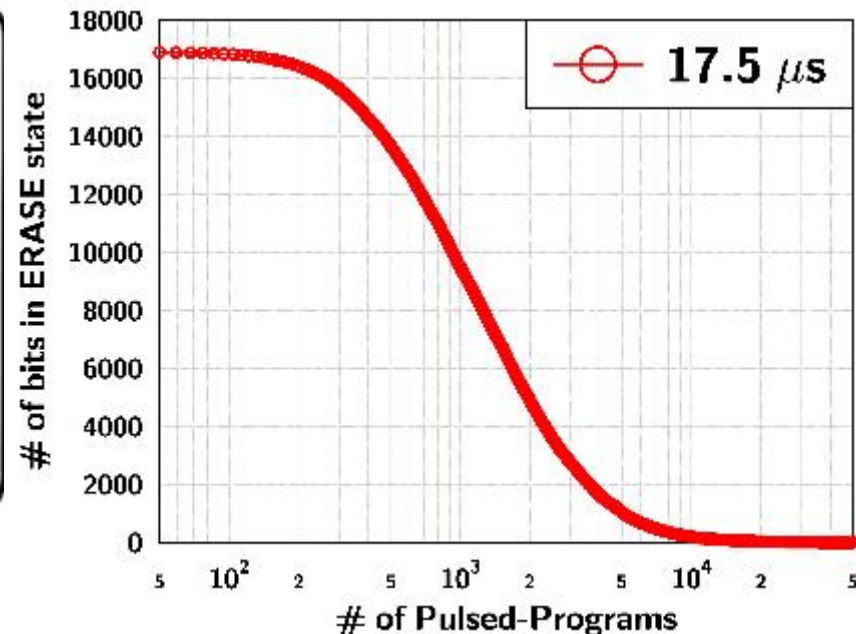
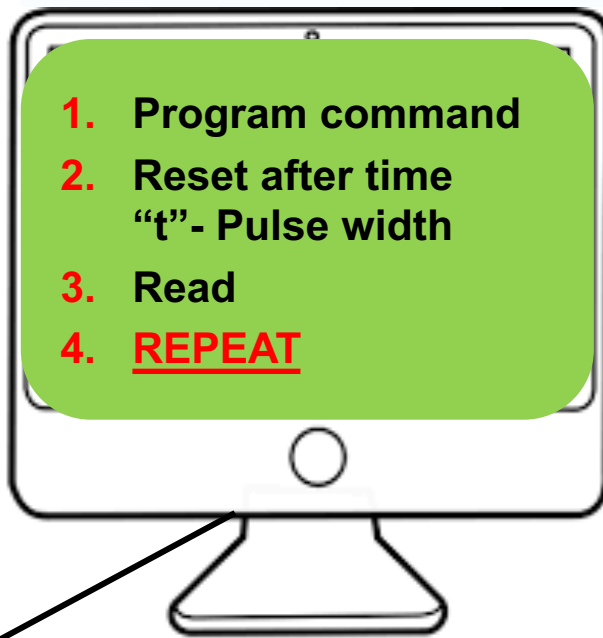


Pulsed/Partial Programming Bit Evaluation Tool

- **Method introduced by Navy Crane demonstrating ability to interrupt NAND programming sequence to create bit level analysis of NAND parts**
- **We have developed this test as part of an internal R&TD task on a commercial NAND tester with a GUI interface to be a readily available tool to evaluate bit level performance for any SLC NAND**
 - **Useful for comparing manufacturers, technology nodes, or even for screening**
 - **FY19 plan is to compare 2D NAND vs 3D NAND in reliability**
- **Identifies outlier “weak” bits which are often the first to fail in reliability and possibly radiation**



How Does Pulsed Programming Work?

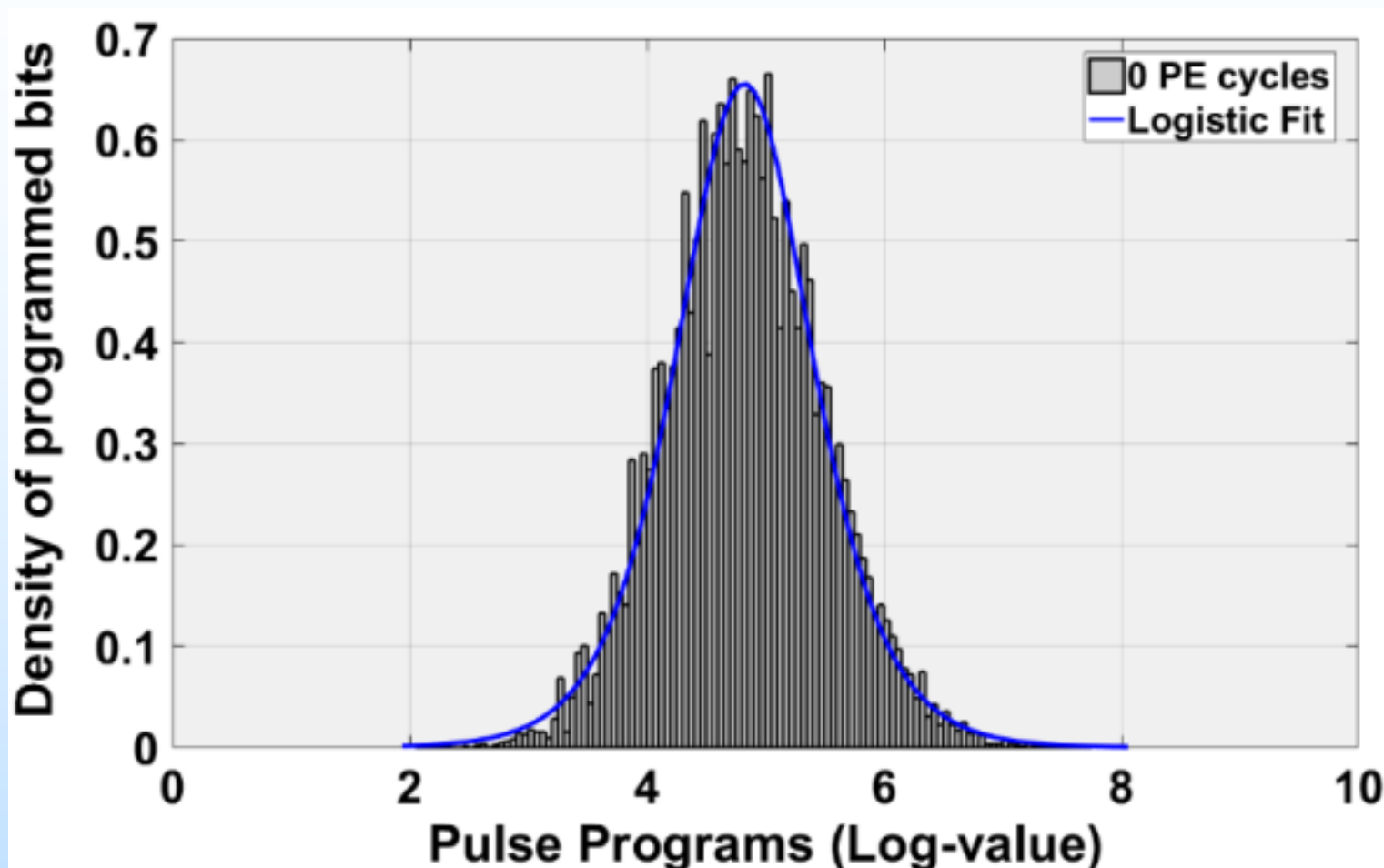


—Tester runs the test through a GUI.

—The resolution of pulse width is limited by the FPGA, which is 50 ns

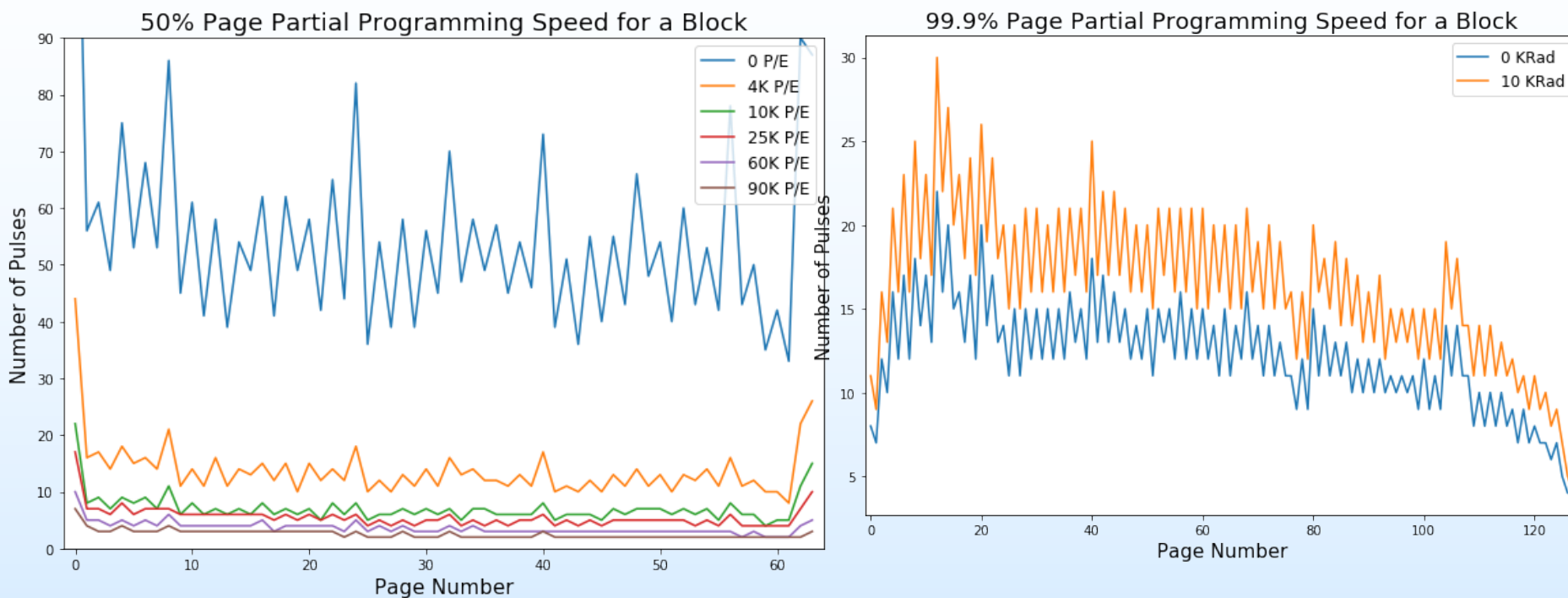


Distribution of bits in programming speed





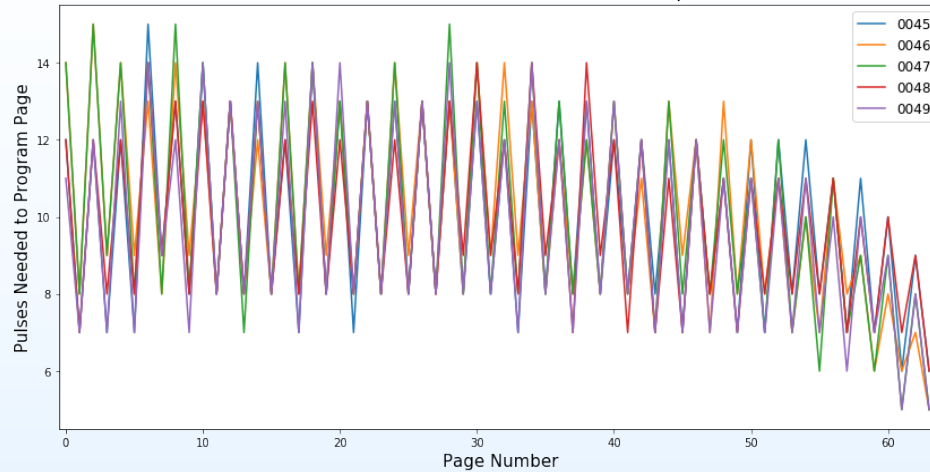
Higher level data- programming speed for a block of pages



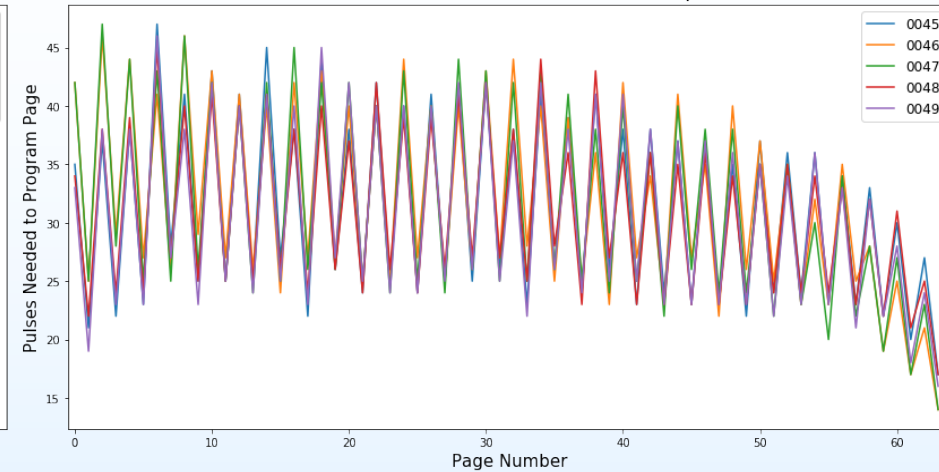


Block level programming data showing the last 5% of the bits require over 90% of the programming time.

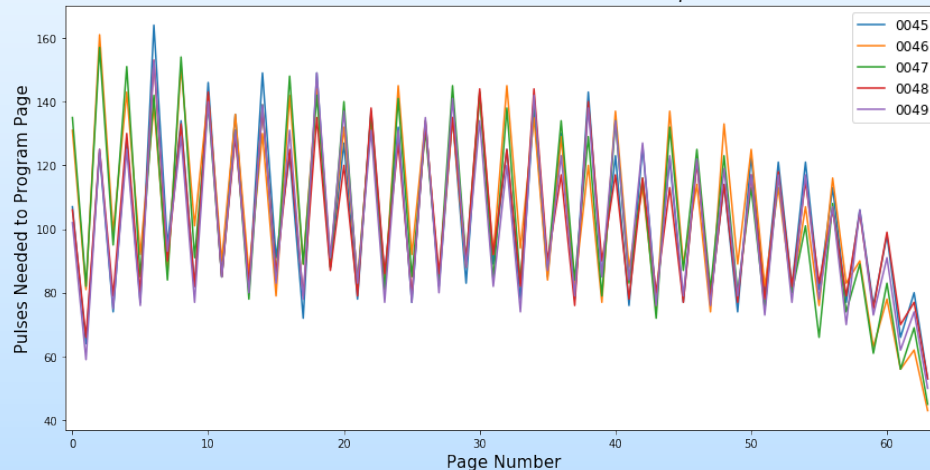
5% Page Programming Time Distribution for a Block via Pulsed Programming
Blocks: 0045 - 0049, Pulsewidth: 25 μ s



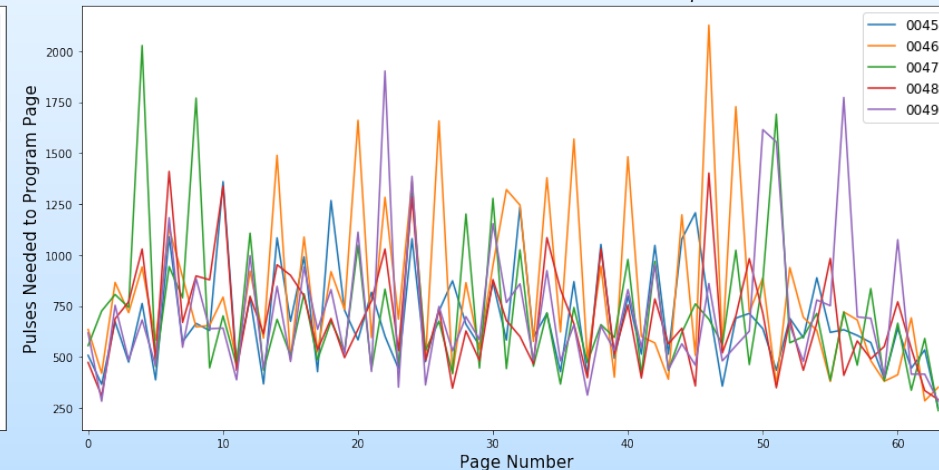
50% Page Programming Time Distribution for a Block via Pulsed Programming
Blocks: 0045 - 0049, Pulsewidth: 25 μ s



95% Page Programming Time Distribution for a Block via Pulsed Programming
Blocks: 0045 - 0049, Pulsewidth: 25 μ s



100% Page Programming Time Distribution for a Block via Pulsed Programming
Blocks: 0045 - 0049, Pulsewidth: 25 μ s

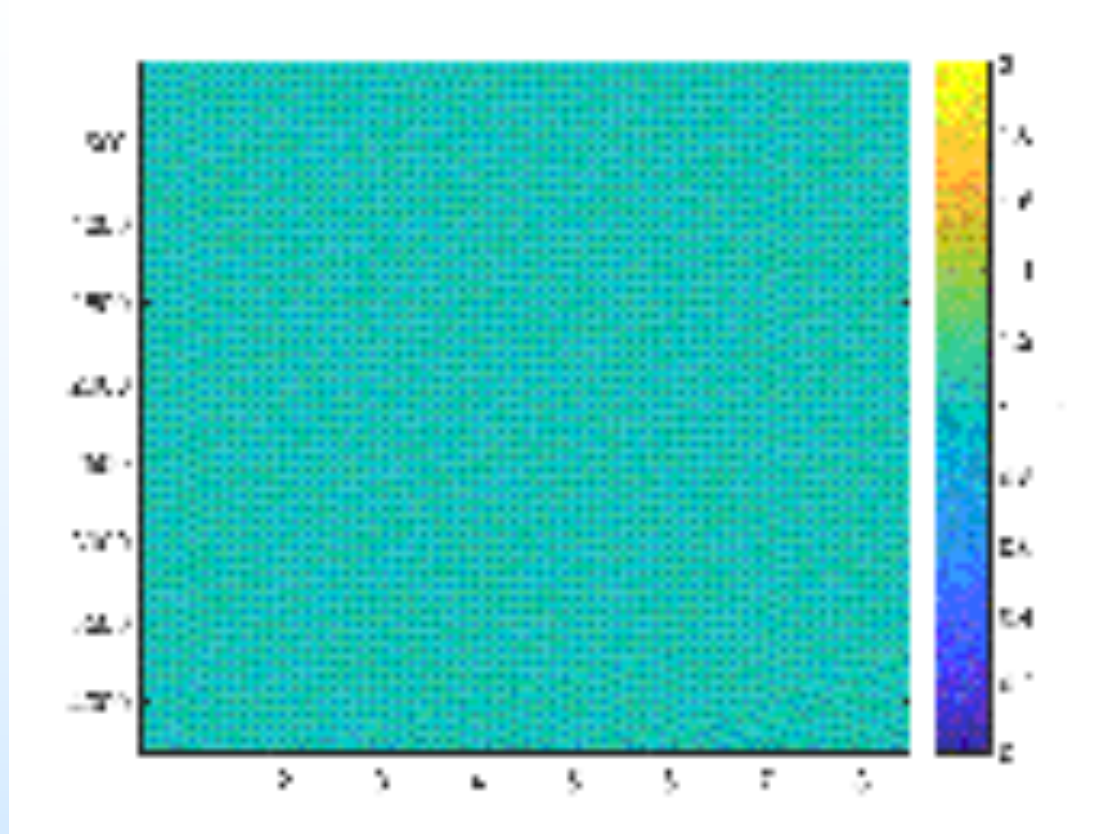


Have also scaled this to look at the full chip by block

To be presented by Jean Yang-Scharlotta at the NEPP Electronic Technology Workshop, June 17-19, 2019.



Bitmaps- Graphical Image of the Statistical Tail

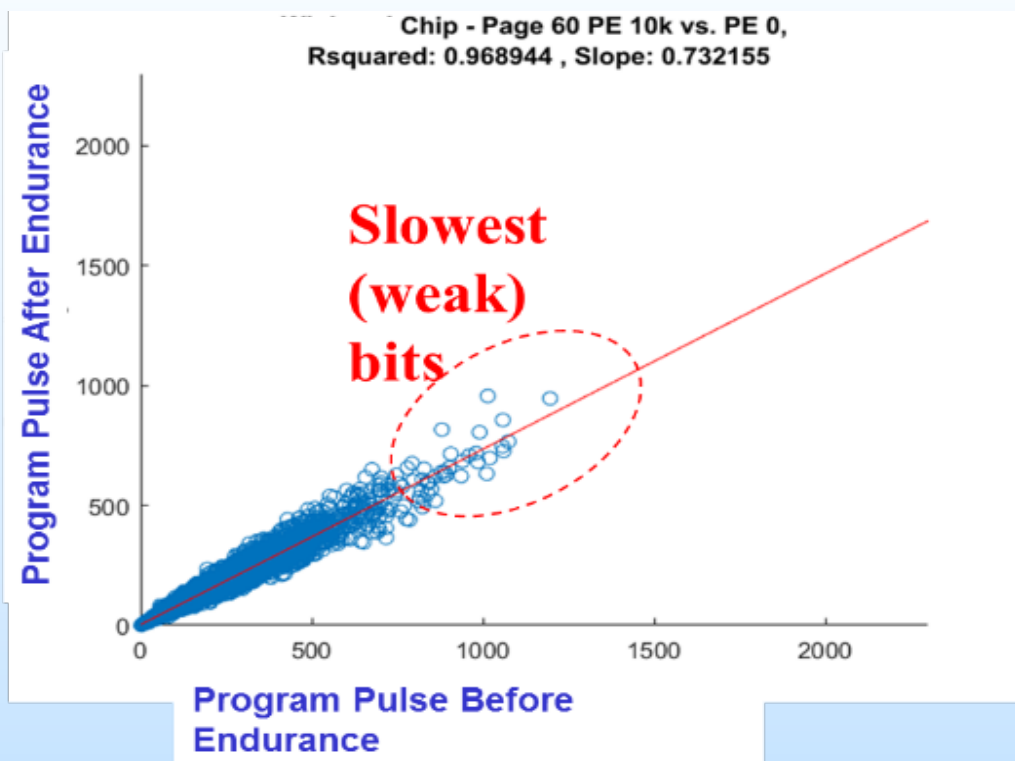


- Weak tail bits take over 90% of the programming time and statistically the first to fail
- We expect this trend to worsen with technology shrink due to lower number of electrons stored = wider statistical variation
- Identifying weak bit trends across part numbers, manufacturer and even parts in a lot allows selection of more reliable parts

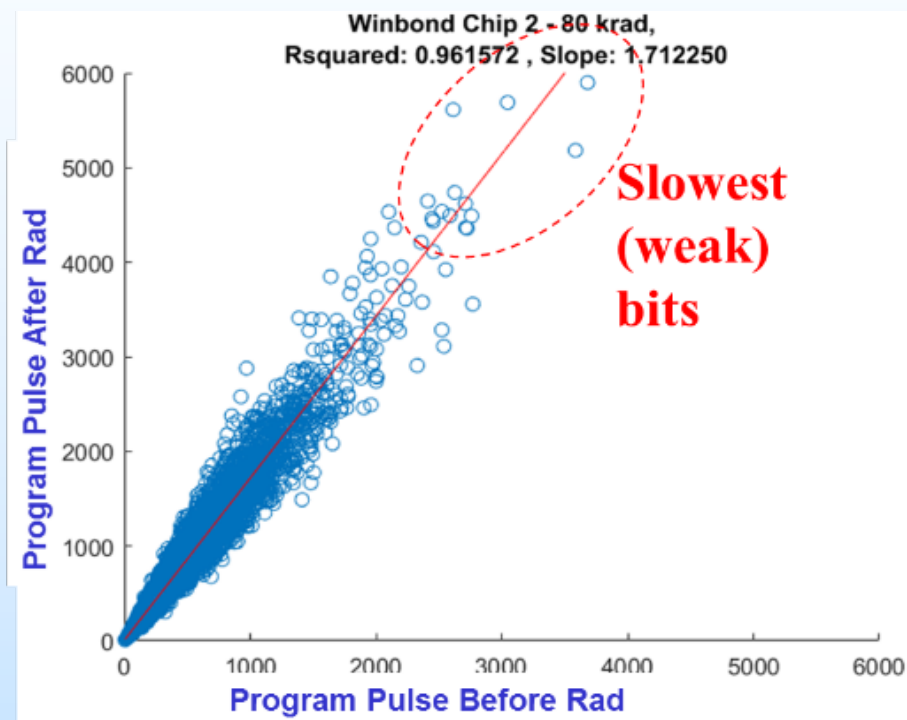


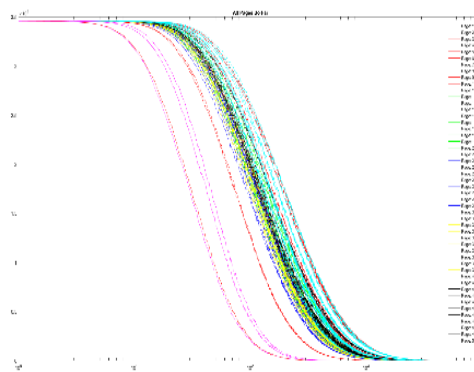
Weak Bits @ t=0 Identifies Reliability and Radiation Vulnerability

Pre/Post Reliability Correlation

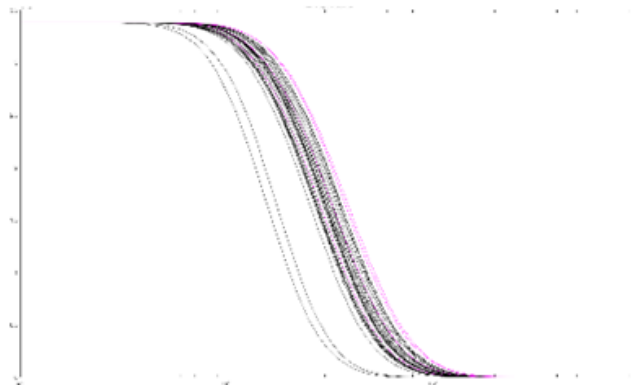


Pre/Post TID Radiation Correlation

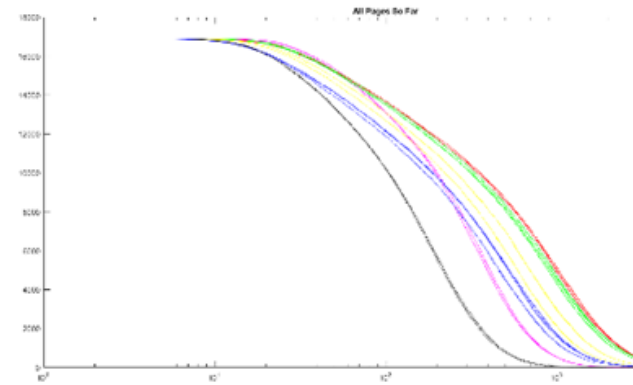




Interrupt program pulses



Interrupt program pulses



Interrupt program pulses

of unprogrammed bits in the page



NAND Flash Future Plans

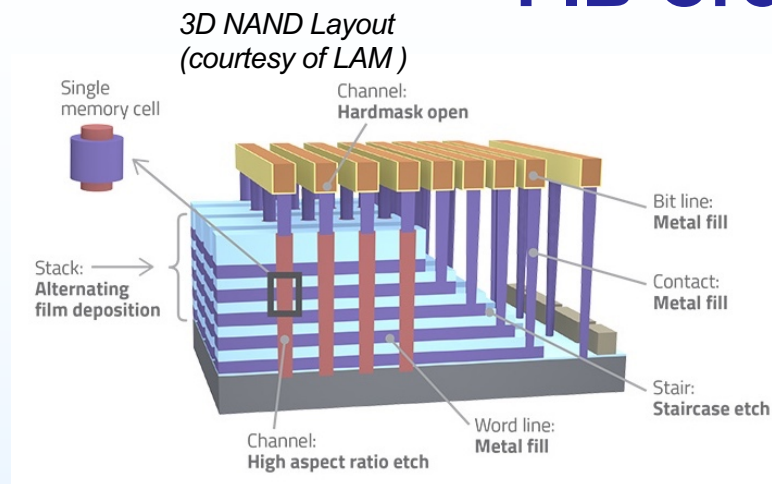
- **For 2019 we will utilize the pulsed programming tool to test Micron and Hynix 3D NAND chips for a comparison of the two fundamental devices used (floating gate versus charge trapping) as well as comparison to 2D NAND reliability performance.**
- **Moving forward, we plan to continue to track new 3D development and test for technology shrink impact on reliability and radiation effects.**



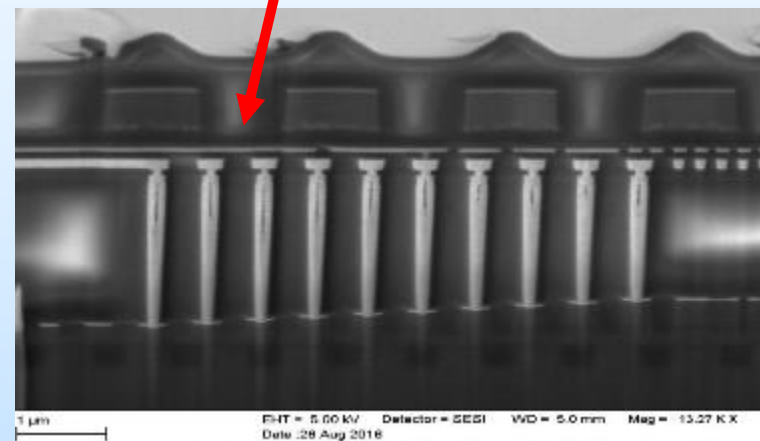
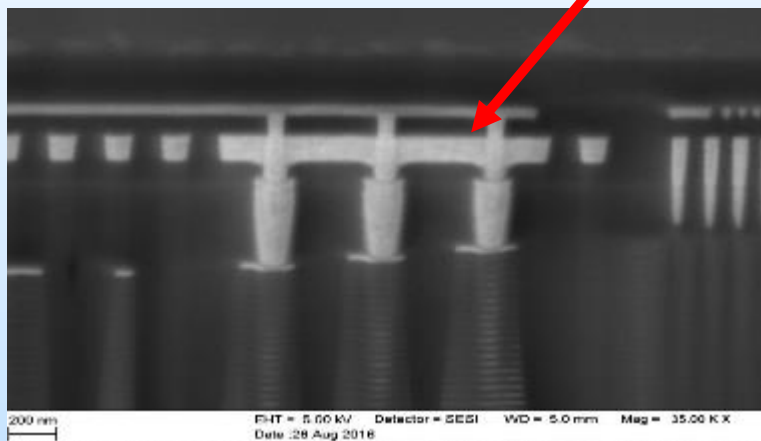
APPENDIX



Hynix 3D 1X nm NAND equivalent FIB Cross-Section- 128Gb



Cross section showing FLASH array transition to periphery. Connections are identified for reference to higher magnification images below. Cross sections were taken along the Y-Axis



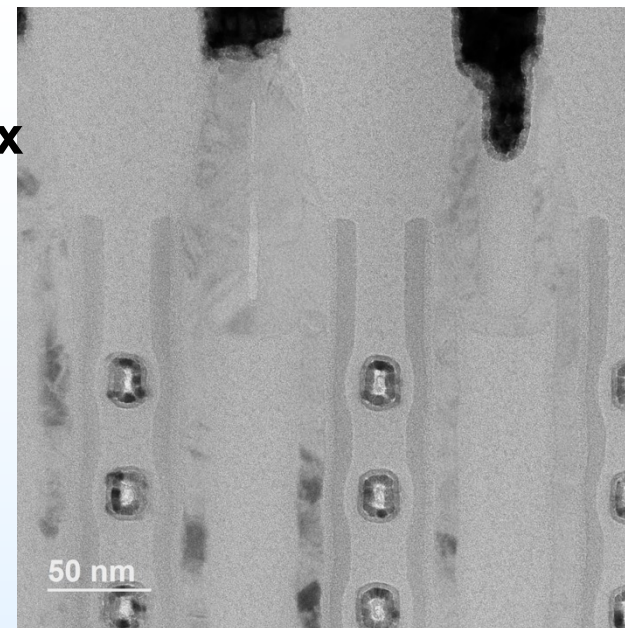
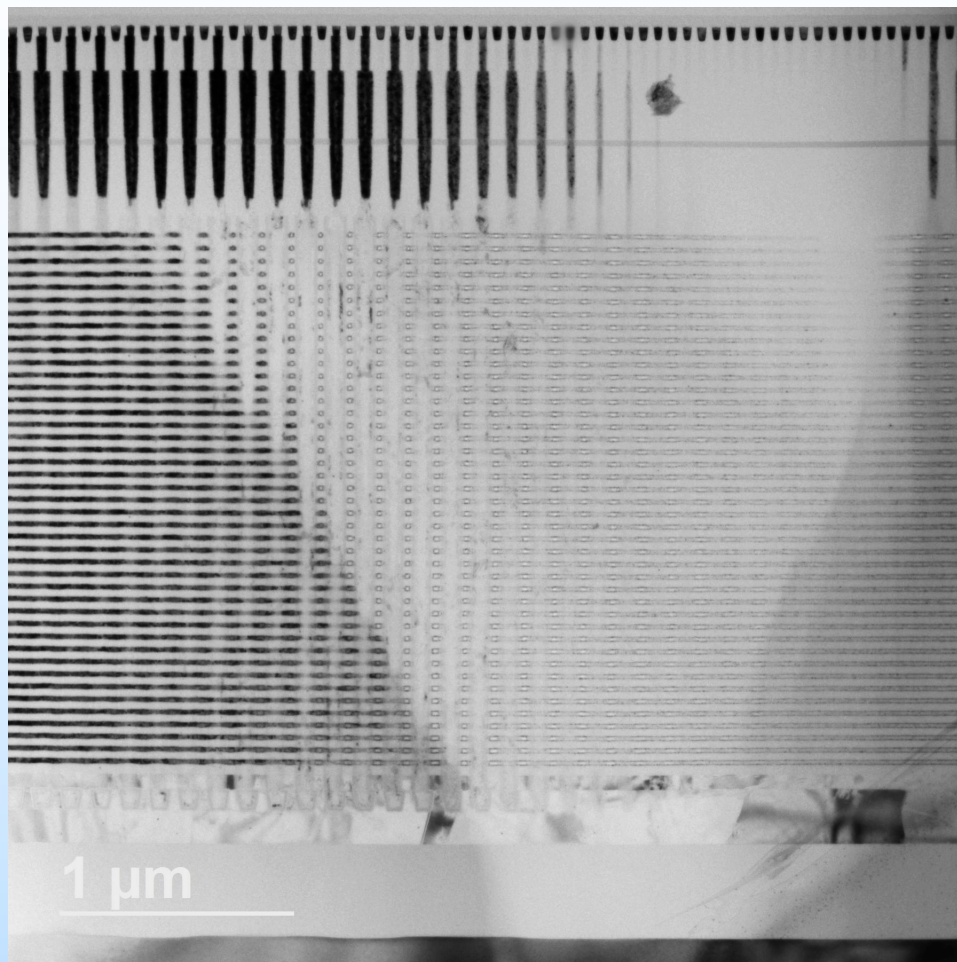
Higher magnification images of array connections

Hynix 3D NAND (128Gb, MLC) initial construction SEM analysis reveals a single die with 3D construction comprising of 40 physical device layers and staircase array edge connection.

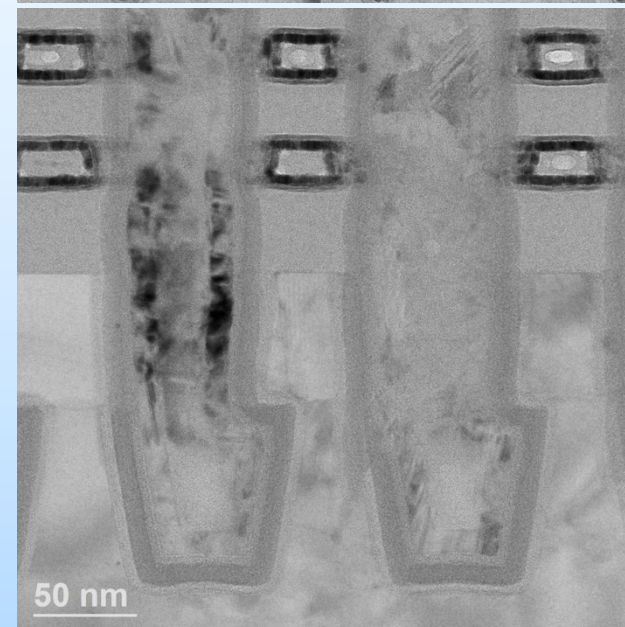


Hynix 3D NAND Y Direction Top and Bottom Details

Overview of the Vertical Stack @ 4500x



Detail View
Top of Array

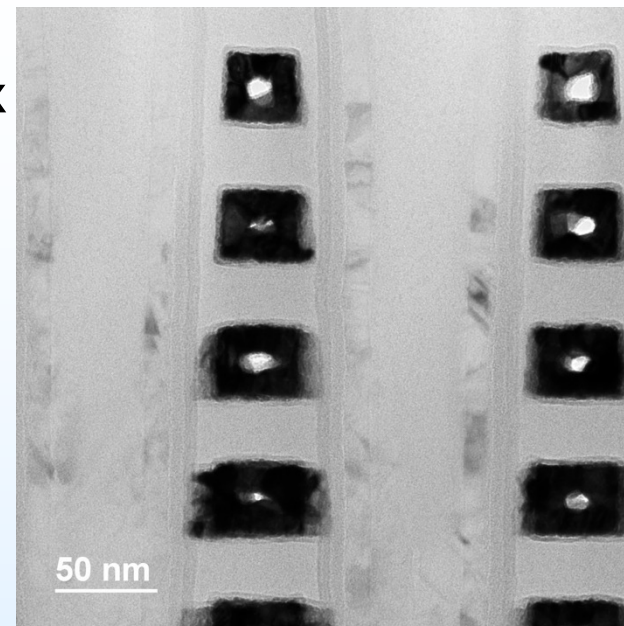
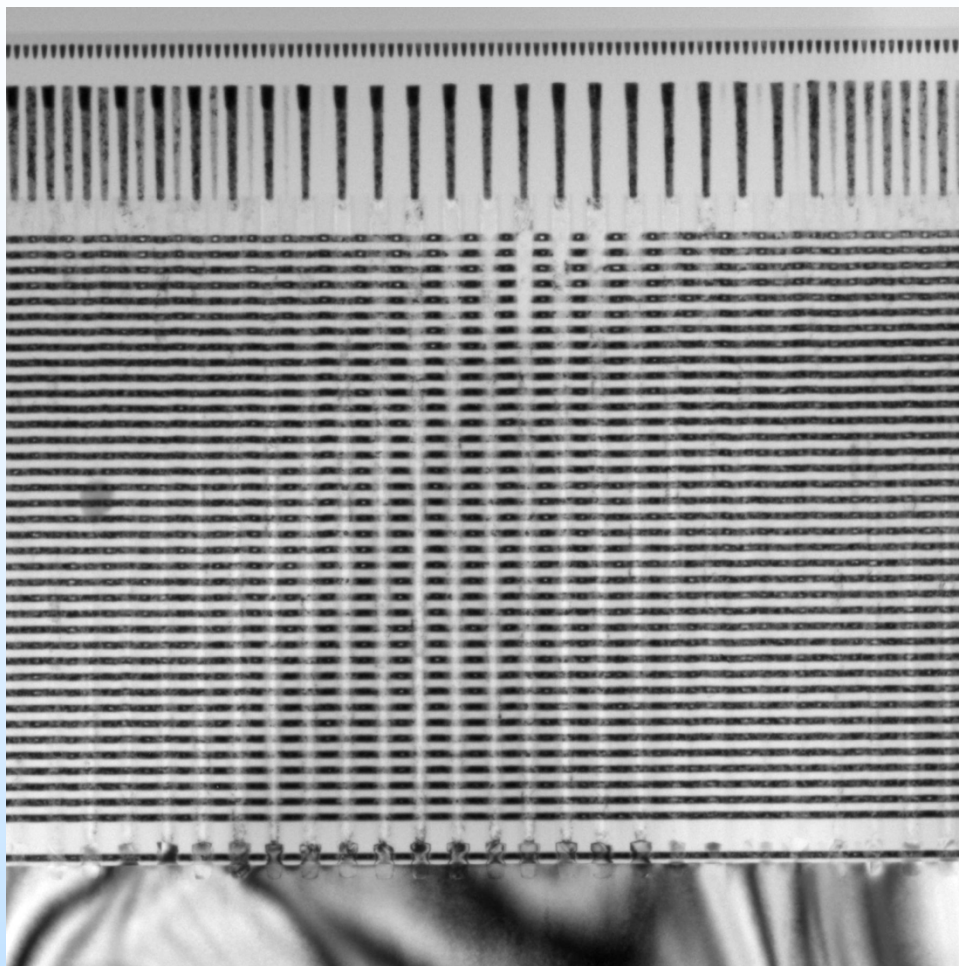


Detail View
Bottom
of Array

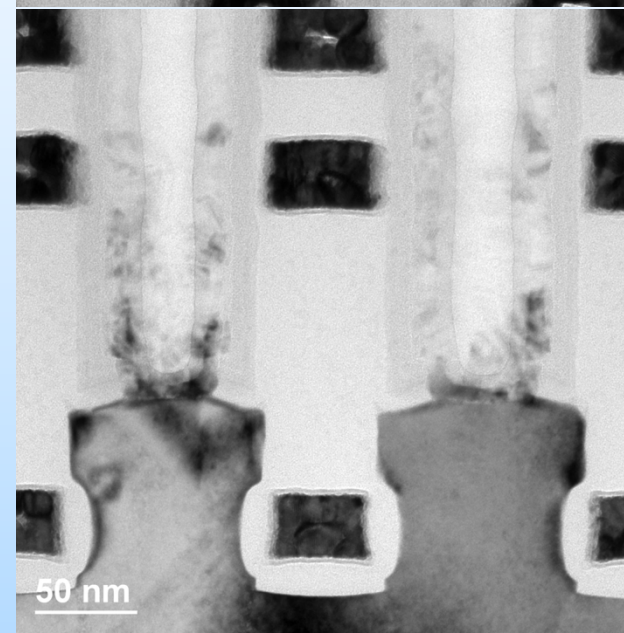


Samsung VNAND 2014 Y Direction Top and Bottom Details

Overview of the Vertical Stack @ 4500x



Detail View
Top of Array



Detail View
Bottom
of Array



1st Device's Ordered: Intel Optane™

3D XPoint™ Technology: An Innovative, High-Density Design

Cross Point Structure

Perpendicular wires connect submicroscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

Non-Volatile

3D XPoint™ Technology is non-volatile—which means your data doesn't go away when your power goes away—making it a great choice for storage.

High Endurance

Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.

Stackable

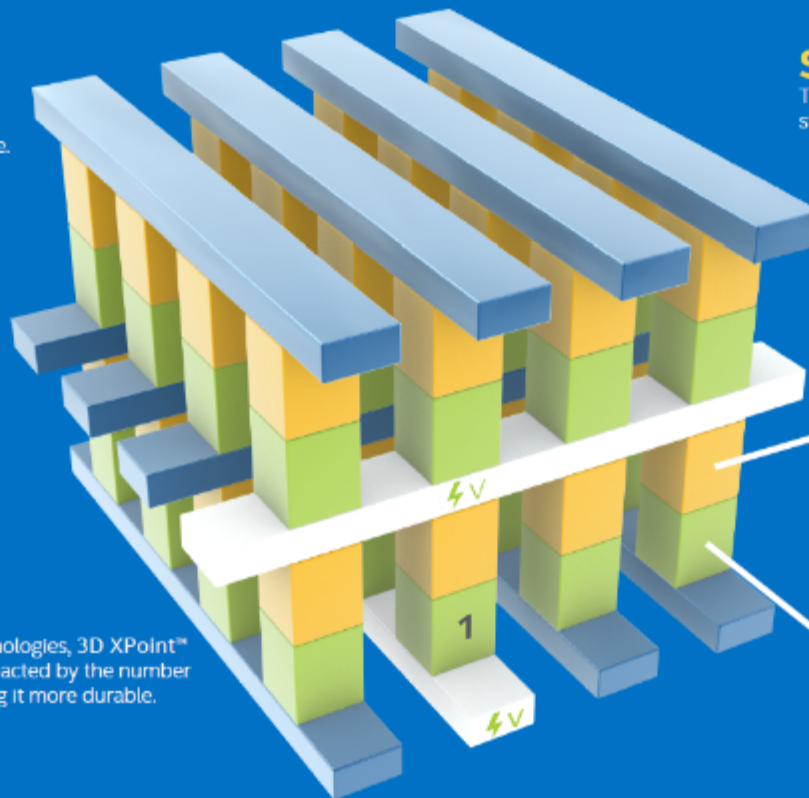
These thin layers of memory can be stacked to further boost density.

Selector

Whereas DRAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

Memory Cell

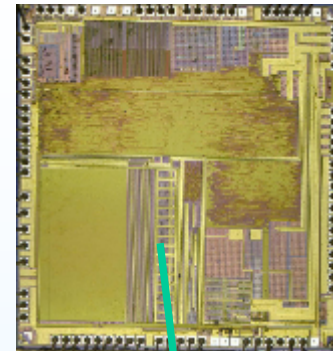
Each memory cell can store a single bit of data.





Resistive Memory (ReRAM)

- **Resistive Memory is a Long Term Storage Candidate Technology**
 - Inherently TID-hard memory elements (Sandia, HP labs, etc)
 - Potential for high density storage memory
- **Panasonic Embedded ReRAM**
 - 512Kb embedded in microcontroller tested 2015/16
 - Pulsed laser testing shows robust cells - but sensitivity in the sense amps
 - Memory reliability similar or better than flash
- **Fujitsu/Panasonic ReRAM**
 - 4Mb stand-alone ReRAM chip
 - Memory cell tech node same as previous embedded memory, but configured for high endurance with EDAC
 - Of interest to understand density scaling of ReRAM without microcontroller
 - Future 45 and 14nm planned by Fujitsu



Panasonic Embedded ReRAM



Location of pulsed laser bit upset sensitivity marked "1"



Fujitsu ReRAM